

FIG. 1A

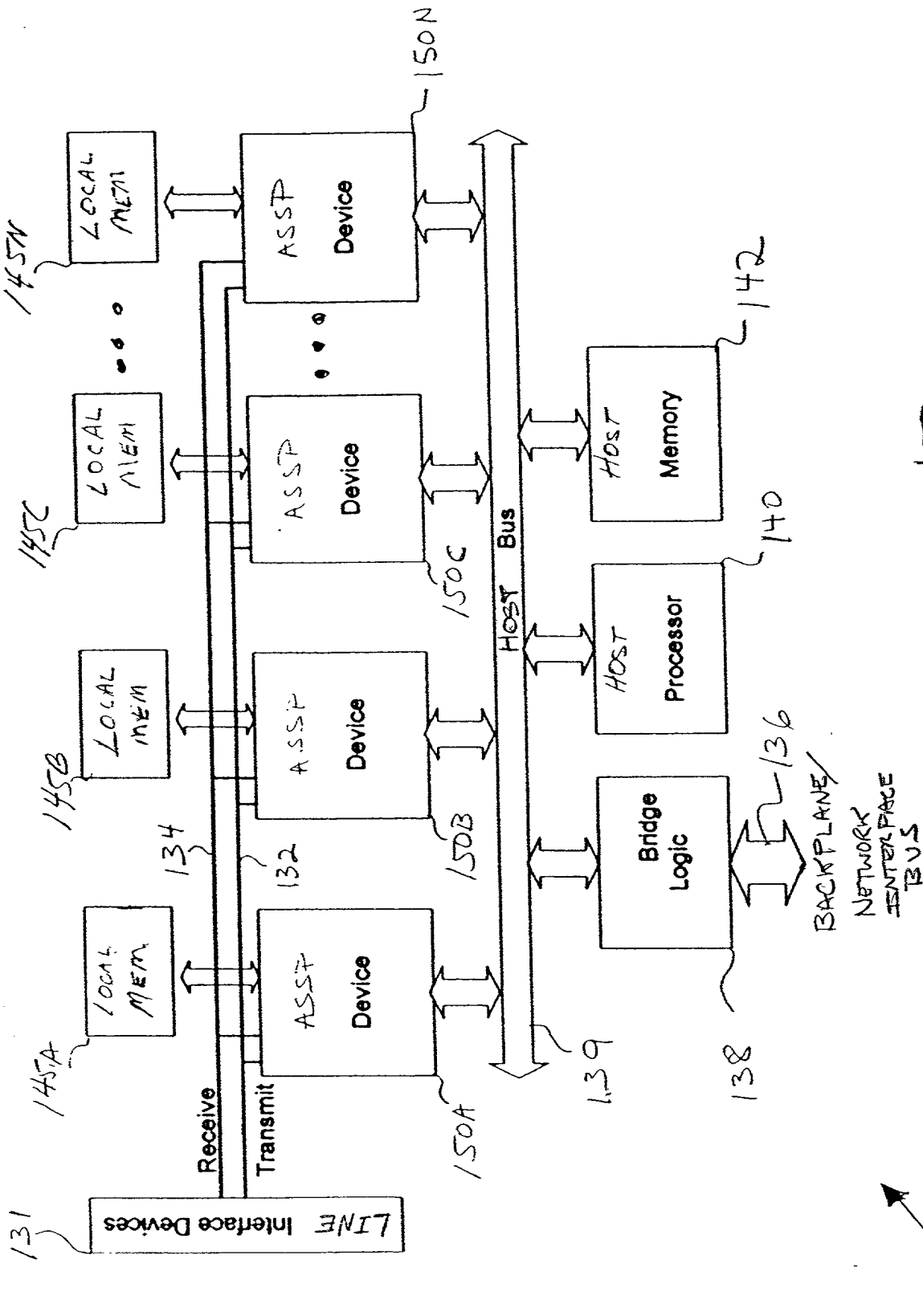


FIG. 1B

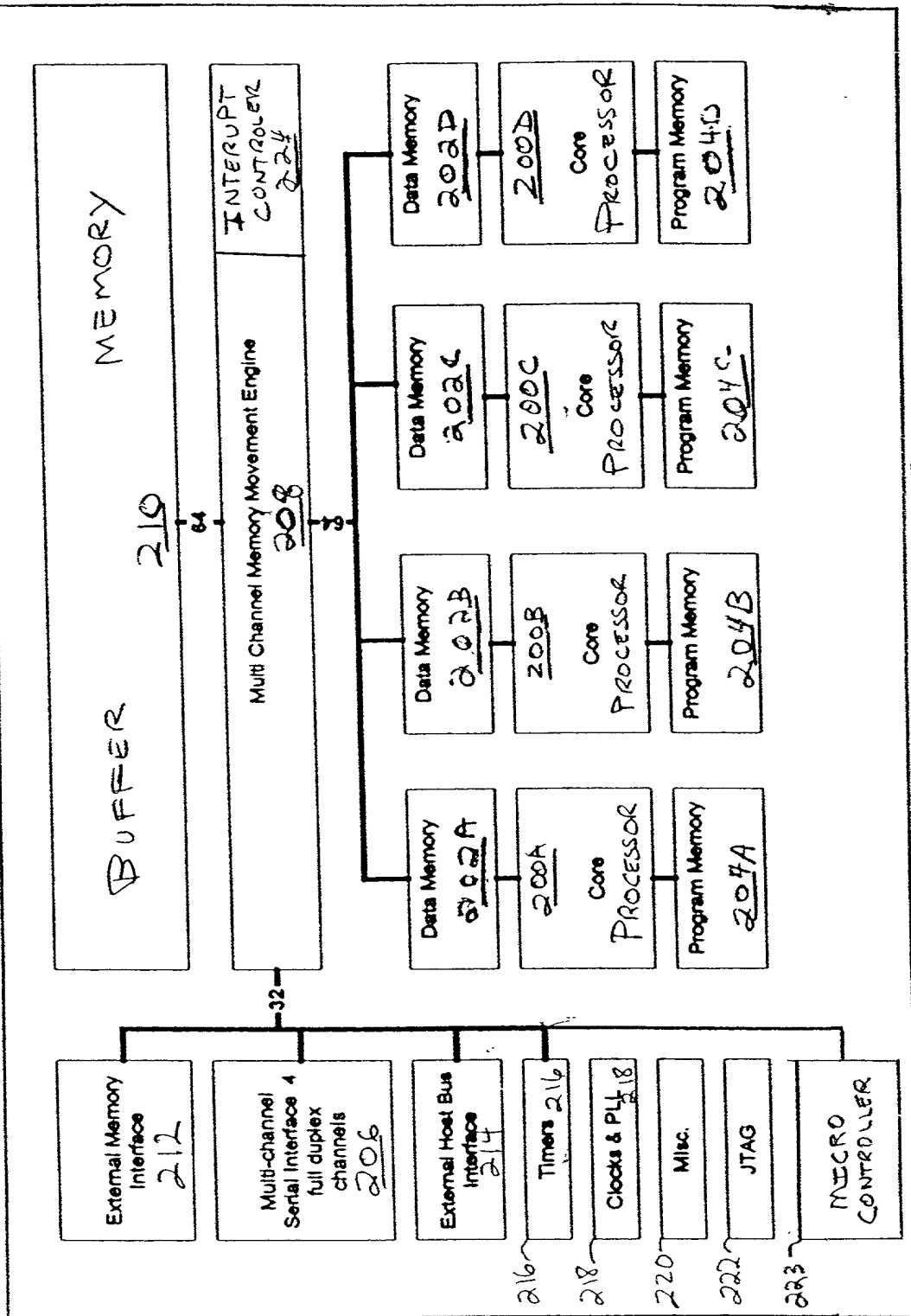


FIG. 2

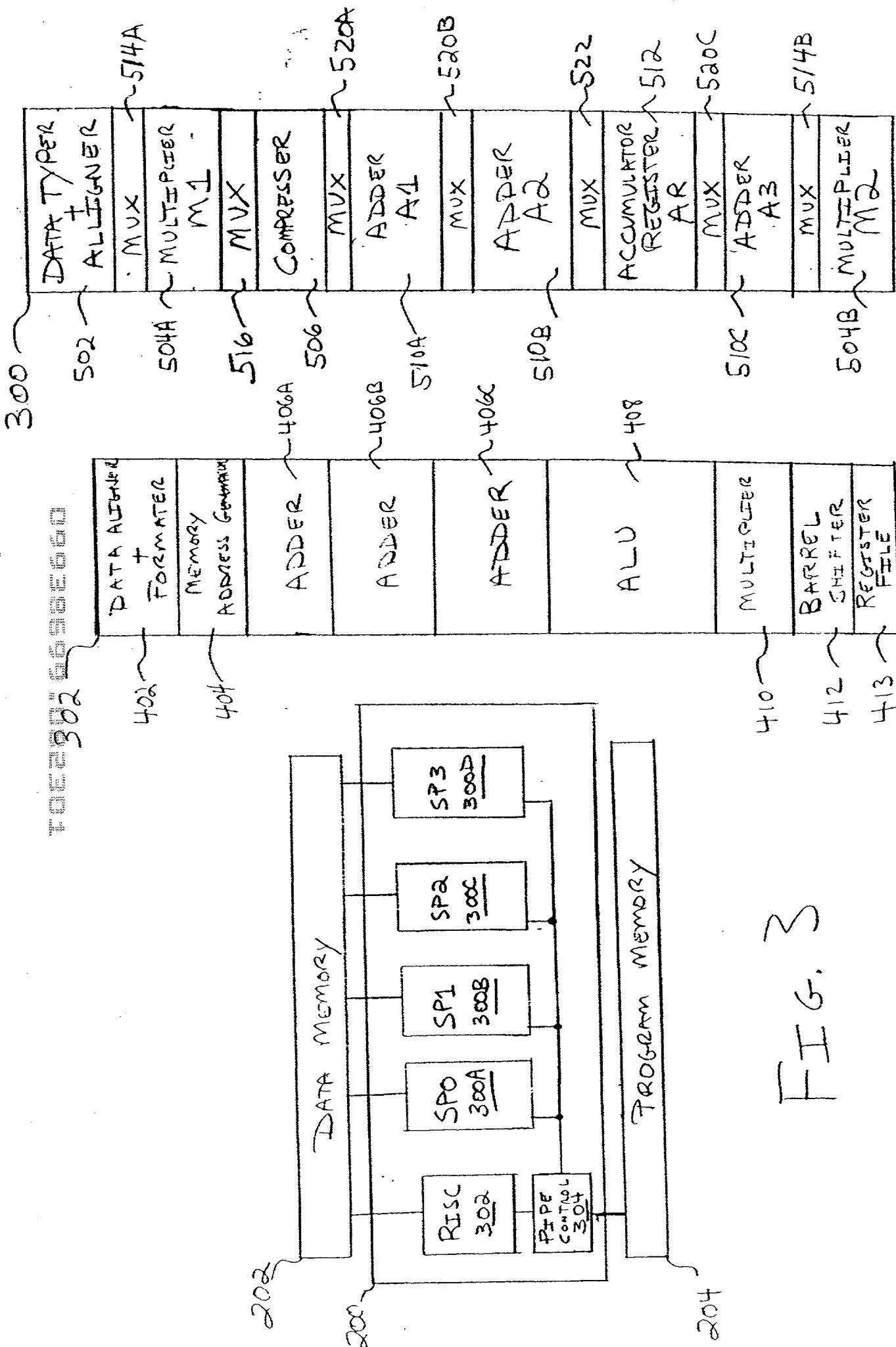


FIG. 3

FIG. 4

FIG. 5A

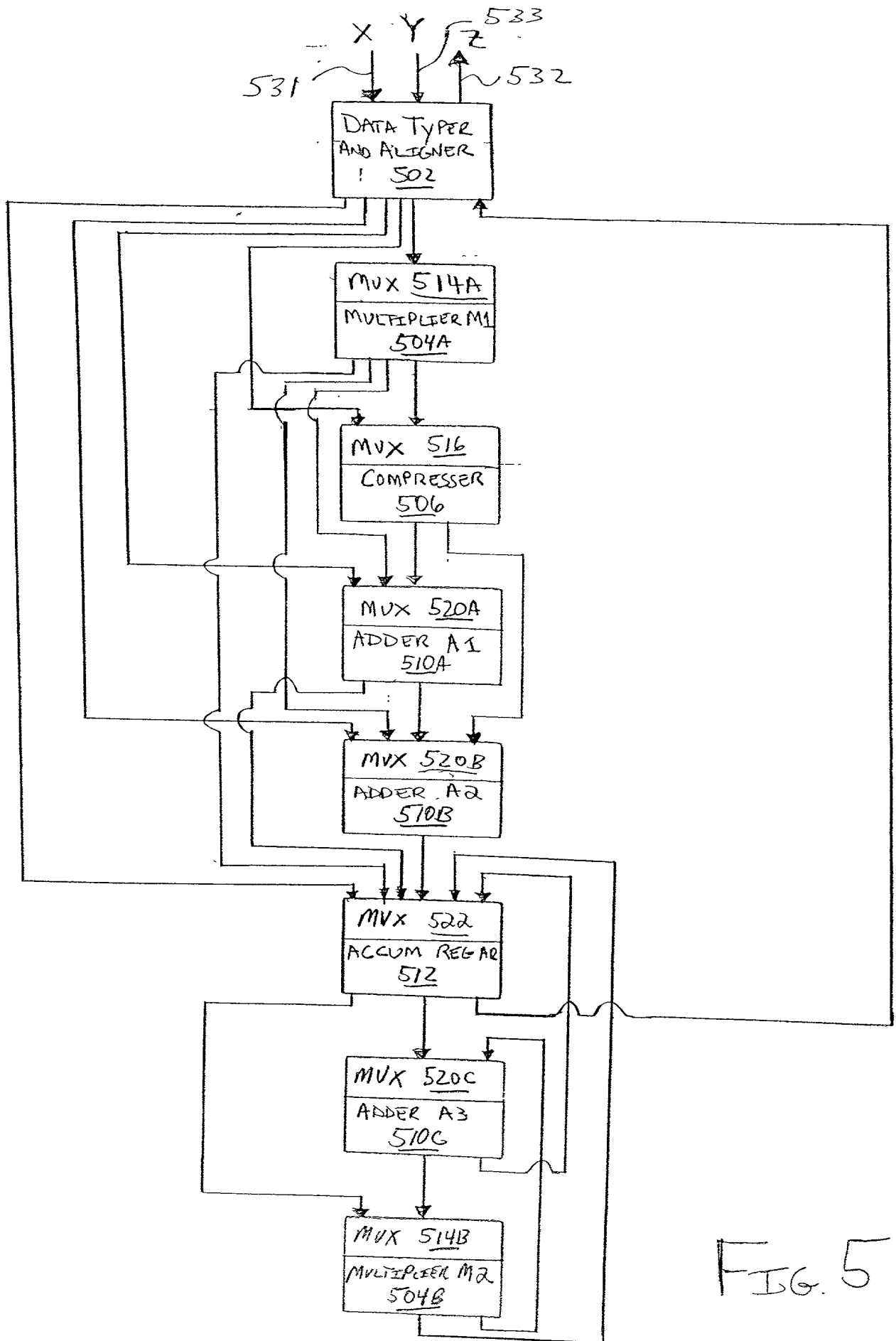
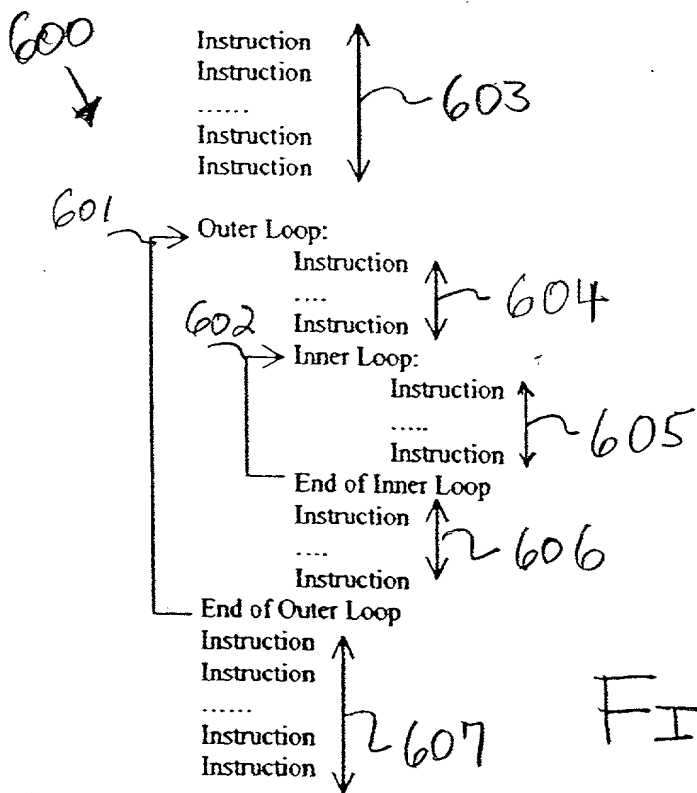


FIG. 5B



610

611	612
MAIN OP	SUB OP
MULT	NOP
ADD	MIN/MAX
MIN/MAX	ADD
NOP	MULT

FIG. 6B

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	PS	S*	SX		SY	V/S	SA	DA	Sub-op	1	Pred	PL	Sxt	Syt	Rnd	S*	S*	S*	0	SA	DA	abs	0	0													
											Nop	0	0	0																									
											Add	0	0	1																									
											Add	0	1	0																									
											Sub	0	1	1																									
											Sub	1	0	0																									
											Min	1	0	1																									
											Min	1	1	0																									
											Max	1	1	1																									

da = +/- sx*sy

da = +/-{sx*sy} + sa

da = +/-{sx*sa} + sy

da = +/-{sx*sy} - sa

da = +/-{sx*sa} - sy

da = min(+/- sx*sy,sa)

da = min(+/- sx*sa,sy)

da = max(+/- sx * sy, sa)

Nop

Add

Add

Sub

Sub

Min

Min

Max

0

0

0

0

1

0

1

0

1

1

0

1

Lt

Lt

Lt

Lt

Gx

Gx

Gx

FIG.

FIG. 6C

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20		
1	0	0	PS	S*	SX					SY					V/S	SA	DA	0	1	0	Add
																	1	0	0	Sub	
																	1	1	0	Min	

$da = +/- (mx * sa) + my$
 $da = +/- (mx * sa) - my$
 $da = \min(+/- mx * sa, my)$

FIG. 6D

Control instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add, sub	L	Pred	0	0	0	0	RX					RY				RZ				0
max, min	L	Pred	0	0	0	0	RX					RY				RZ				0
Shift	L	Pred	0	0	0	1	RX					U14				RZ				U11 R/L
Logic	L	Pred	0	1	0	0	RX					RY				RZ				&1, &1
Mux	L	Pred	0	1	1	0	RX					RY				RZ				Pd 0
mov	L	Pred	0	1	1	1	RX					DZ				Rx/Dz1	0	0	0	1
addi	L	Pred	0	1	1	1	Sl4					DZ				x	1	1	0	0
mov2arg	L	Pred	0	1	1	1	RX				unit	ereg				gd	type	1	0	1
	L	Pred	0	1	1	1	RX					DZ1				DZ2				1
bits	L	Pred	1	0	0	0	U14 POS					RZ				Rz1				U14
set2bits	L	Pred	1	0	0	0	U14 POS					RZ				Rz1				U12
Setbit	L	Pred	1	0	0	0	U14 POS					RZ				Rz1				U11
Movi	L	Pred	1	0	0	0	Sl8									RZ				1
Call	L	Pred	1	0	1	0				Sl9										0
Loop	L	Pred	1	0	1	0				Sl9										1
Loopi	L	Pred	1	0	1	0				U15, Lcount						U15, Lsize				U12, Lst
Test	L	Pred	1	0	1	0	RX					x	x	x	x	x				0
Andp, orp	L	Pred	1	0	1	0	RX					x	x	x	x	x				0
Load	L	Pred	1	1	1	1	MX					RZ				Ext				1
Store	L	Pred	1	1	1	1	MZ					RX				Ext				1
eLoad	L	Pred	1	1	1	1	MX					RZ				1	1	1	0	0
eStore	L	Pred	1	1	1	1	MZ					RX				1	1	1	0	0
Extended	L	Pred	1	1	1	1														0
Logic2	L	Pred	1	1	1	1	RX					RY/RZ				Rx1				1
mov-erg	L	Pred	1	1	1	1	unit			ereg		RZ				gd				0
Crp	L	Pred	1	1	1	1	RX					RZ				sm				0
Parity	L	Pred	1	1	1	1	RX					PZ				O/E				0
Stm	L	Pred	1	1	1	1	MZ					RX				1	1	0	1	1
Abs	L	Pred	1	1	1	1	RX					RZ				0	0	1	1	1
Nag	L	Pred	1	1	1	1	RX					RZ				0	1	1	1	1
step	L	Pred	1	1	1	1	RX					RZ				1	0	1	1	1
J & Set	L	Pred	1	1	1	1	RX					PZ				0	1	1	1	1
Reserved	L	Pred	1	1	1	1														1
Return	L	Pred	1	1	1	1	Pred			l-clt		0	1	0	1	1	1	1	1	1
Zero-ac	L	Pred	1	1	1	1				ac #		1	1	0	1	1	1	1	1	1
eSync	L	Pred	1	1	1	1				RZ		0	1	1	1	1	1	1	1	1
Swi	L	Pred	1	1	1	1				U13		0	1	1	1	1	1	1	1	1
Nop	L	Pred	1	1	1	1				U13		1	1	1	1	1	1	1	1	1

<Blt1, Blt9-8> == U15 (Shift Amount)

<Blt3, Blt13-10> == U15 :POS

FIG. 6 F

MAC;

[illegible]

MUL-NOP
MUL-ADD
MUL-EXT
MUL-MUL

ARITH:

[illegible]

EXT.

[illegible]

LOGIC:

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		Pred				opcode								SX						SY								DZ											

SHIFT.

[illegible]

Immediate:

Imm32																																Imm16															
Group								DZ								SX								DZ								Subop															
opcode																																															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								

Test:

[illegible]

Branch:

[illegible]

Misc:

FIG. 6H

7-bit specifier: Parallel Store, Parallel Load in DSP Instructions

	6	5	4	3	2	1	0
MIR	0	0	0				
	0	0	0				SPR, a0-a15
	0	0	1				reserved
	0	1	0				ac-names
	0	1	1				qbr, r0-r15
	1	0					off
	1	1					pir (r0) to (r15)
	1	1					offset, U14
							pir

	Always postupdate	Always preupdate
Mem(ptr) ptr == idx		ptr: p14, p15
Mem(ptr + idx)		

6-bit specifier DSP instructions

5	4	3	2	1	0
M/R					
0	0	ac-names			
0	1	gpr r0-r15			
1	1	pvr (r0 to r15) off			

Always postupdate

60610 RISC Instructions

4	3	2	1	0
---	---	---	---	---

4-bit specifier

3	2	1	0
pdr. r0-r15			
pdr. (r0-r7) off			
ereg			

- RISC Instructions
- 20-bit DSP Instructions
- 20-bit Shadow DSP Instructions

AR		2001 SHROU OF THE COUNTY		2001		2002		2003		2004		2005		2006		2007		2008		2009		2010		2011		2012		2013		2014		2015		2016		2017		2018		2019		2020		2021		2022		2023		2024		2025		2026		2027		2028		2029		2030		2031		2032		2033		2034		2035		2036		2037		2038		2039		2040		2041		2042		2043		2044		2045		2046		2047		2048		2049		2050		2051		2052		2053		2054		2055		2056		2057		2058		2059		2060		2061		2062		2063		2064		2065		2066		2067		2068		2069		2070		2071		2072		2073		2074		2075		2076		2077		2078		2079		2080		2081		2082		2083		2084		2085		2086		2087		2088		2089		2090		2091		2092		2093		2094		2095		2096		2097		2098		2099		2100		2101		2102		2103		2104		2105		2106		2107		2108		2109		2110		2111		2112		2113		2114		2115		2116		2117		2118		2119		2120		2121		2122		2123		2124		2125		2126		2127		2128		2129		2130		2131		2132		2133		2134		2135		2136		2137		2138		2139		2140		2141		2142		2143		2144		2145		2146		2147		2148		2149		2150		2151		2152		2153		2154		2155		2156		2157		2158		2159		2160		2161		2162		2163		2164		2165		2166		2167		2168		2169		2170		2171		2172		2173		2174		2175		2176		2177		2178		2179		2180		2181		2182		2183		2184		2185		2186		2187		2188		2189		2190		2191		2192		2193		2194		2195		2196		2197		2198		2199		2200		2201		2202		2203		2204		2205		2206		2207		2208		2209		2210		2211		2212		2213		2214		2215		2216		2217		2218		2219		2220		2221		2222		2223		2224		2225		2226		2227		2228		2229		2230		2231		2232		2233		2234		2235		2236		2237		2238		2239		2240		2241		2242		2243		2244		2245		2246		2247		2248		2249		2250		2251		2252		2253		2254		2255		2256		2257		2258		2259		2260		2261		2262		2263		2264		2265		2266		2267		2268		2269		2270		2271		2272		2273		2274		2275		2276		2277		2278		2279		2280		2281		2282		2283		2284		2285		2286		2287		2288		2289		2290		2291		2292		2293		2294		2295		2296		2297		2298		2299		2300		2301		2302		2303		2304		2305		2306		2307		2308		2309		2310		2311		2312																																																																																																																																																																																																																																																																																																																																																																																																		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																					

ac-names

0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0	0	1
2	0	0	0	0	1	0	1	0	0	1
3	0	0	0	0	0	1	0	0	1	1

SPR.

```
gpr-type
ereg-type
hu-ctl
pls-ctl
ob-ctl
loop-ctl
pcr
status
```

A0 (u8 type, SIMD)

ereg-namoz

0	0	1	1	0	1	0	1	0	1	0	1	0
1	0	0	1	0	1	0	1	0	0	1	0	1
2	0	0	0	1	0	1	0	1	0	1	1	1
3	0	0	0	0	0	0	1	1	1	1	1	1

FIG. 6
I

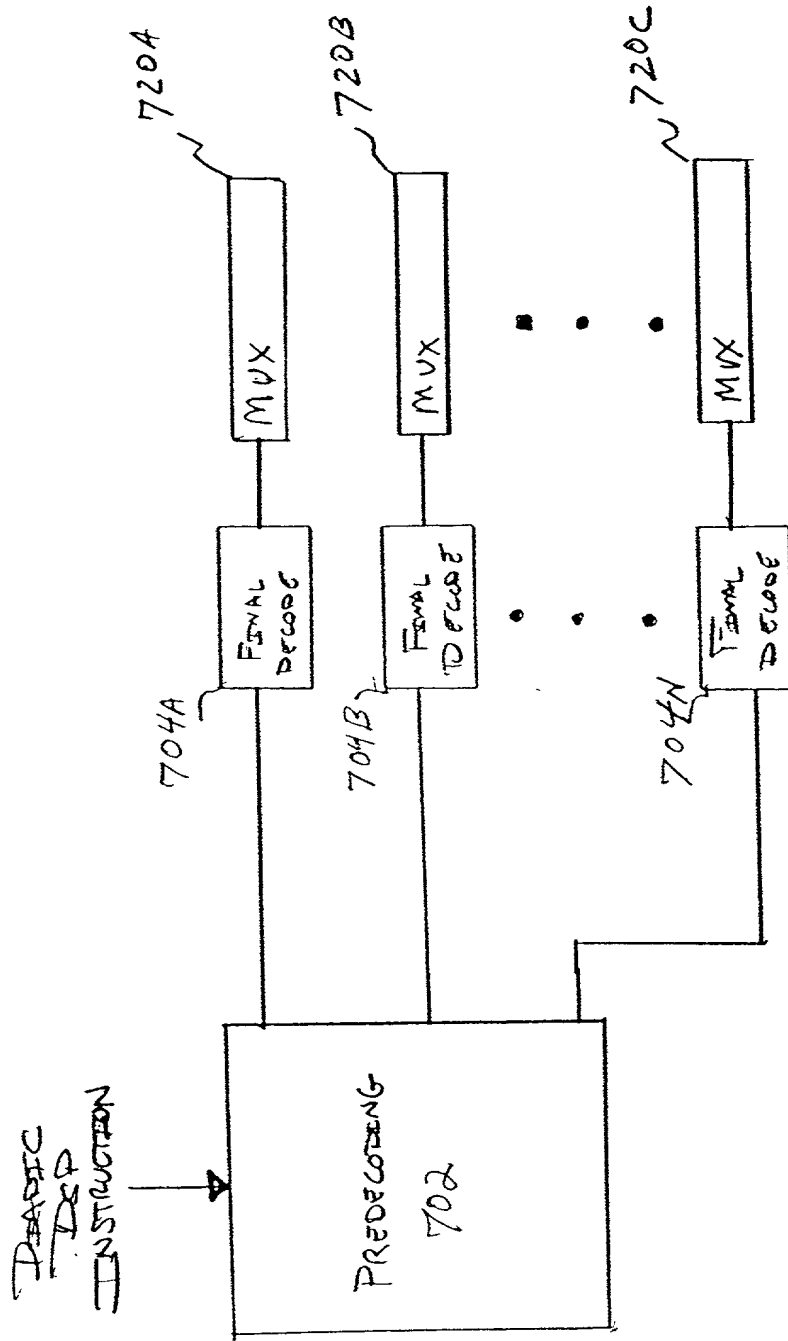


FIG. 7

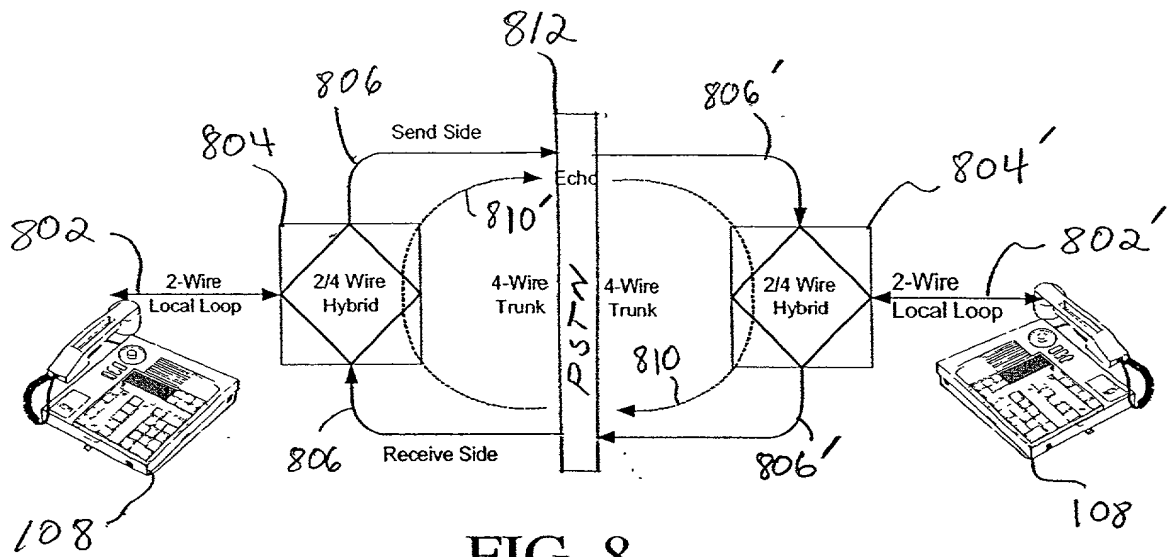


FIG. 8
(PRIOR ART)

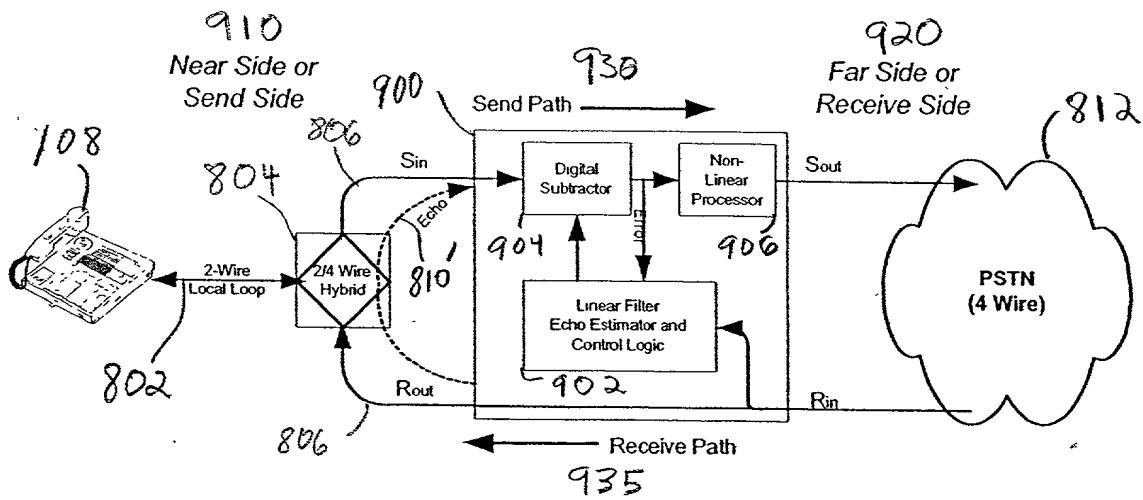


FIG. 9
(PRIOR ART)

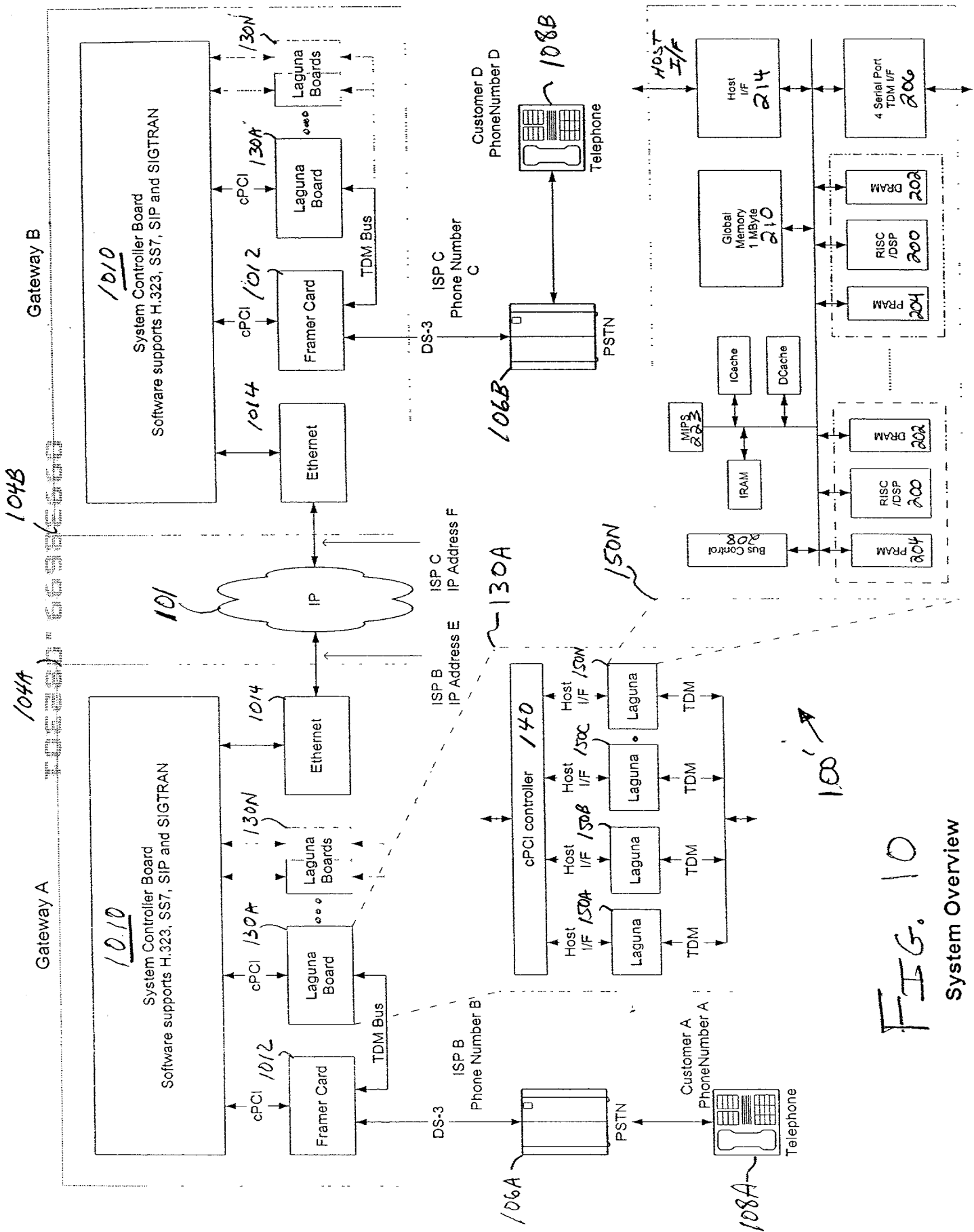


FIG. 10
System Overview

FIG. 11A

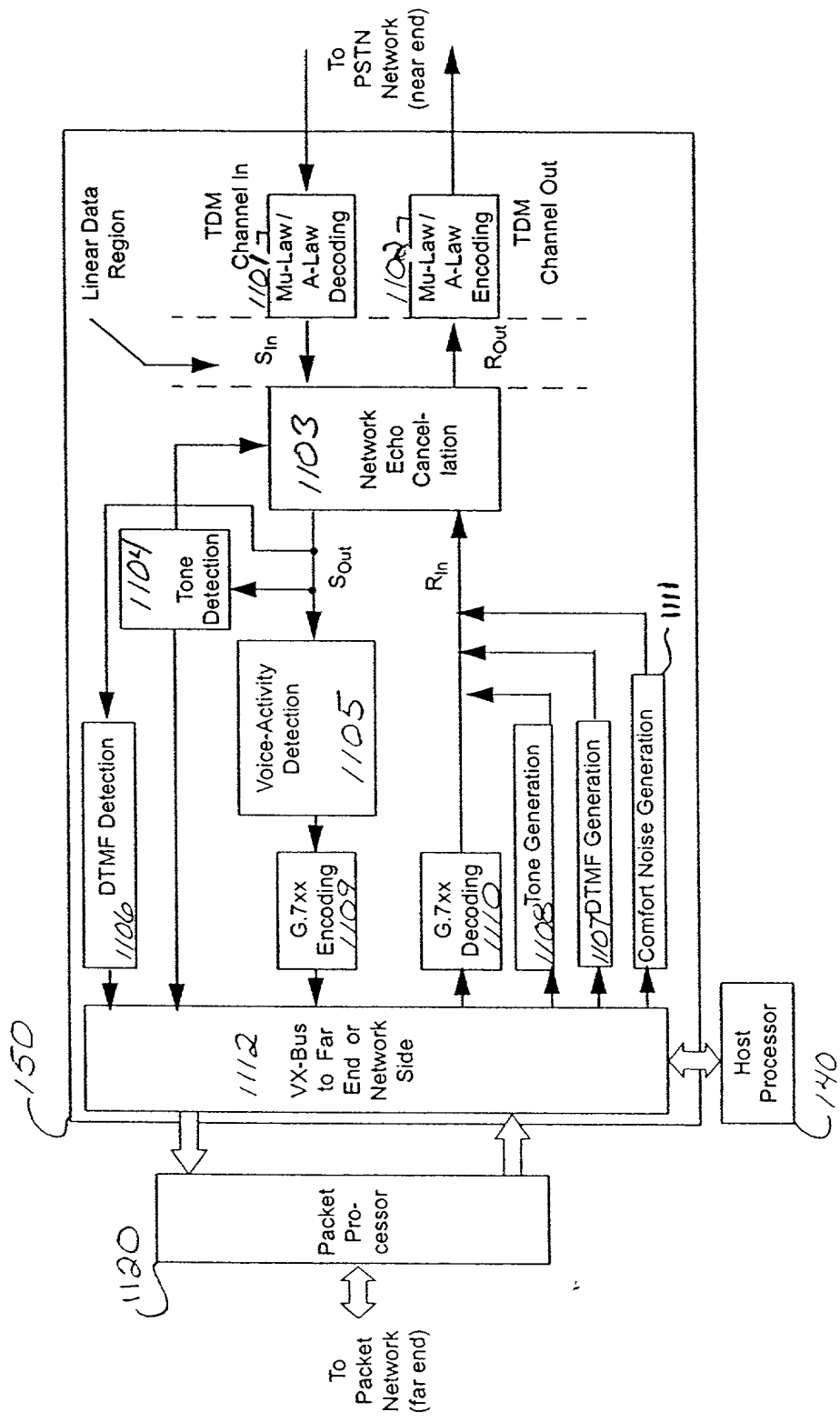


FIG. 11A

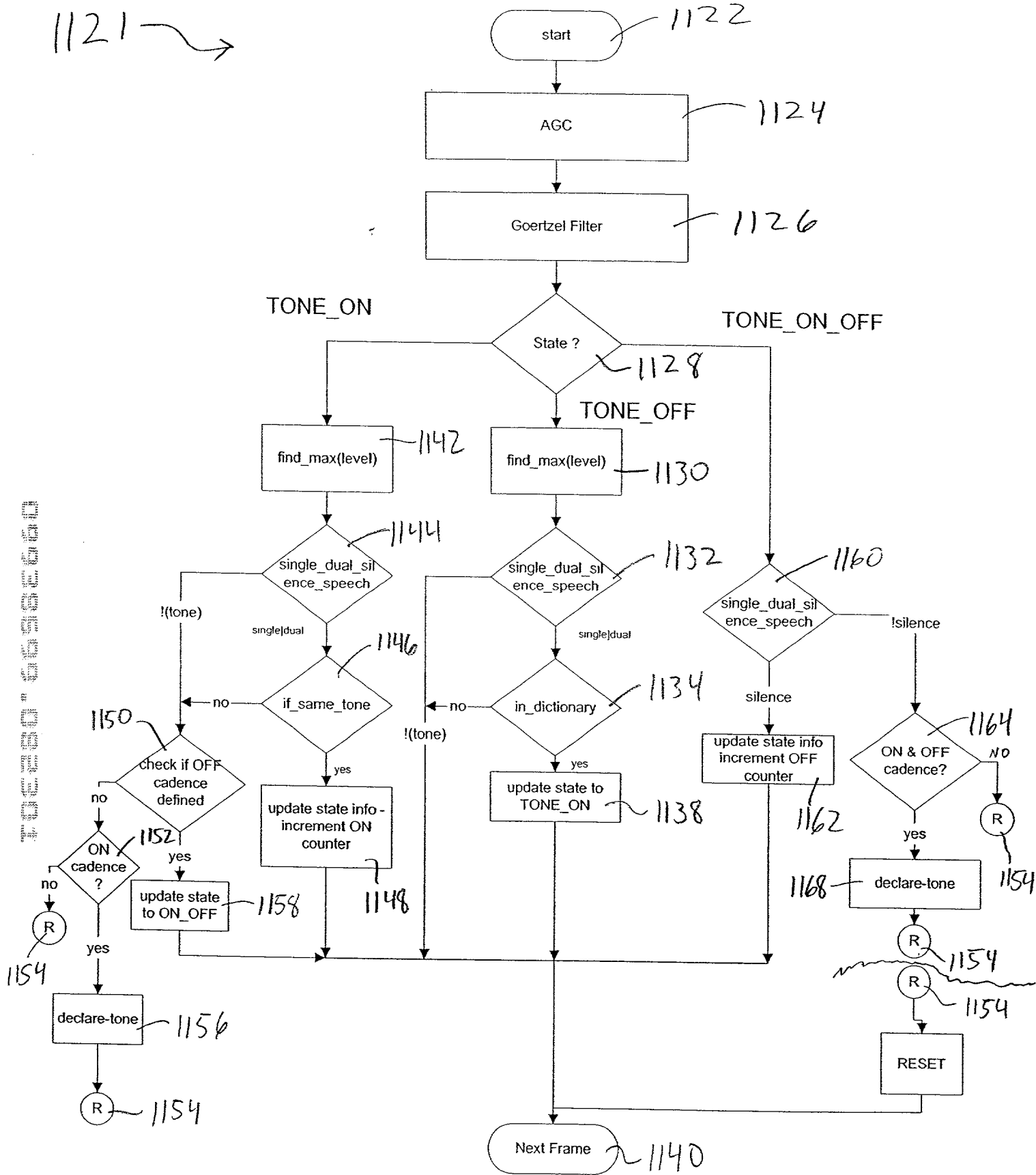


FIG. 11B

Exemplary Filter coefficients for Goertzel Filter

frequency	$\cos(2\pi f_1/f_s)$	frequency index
350	31536	0
400	31163	1
425	30958	2
440	30829	3
480	30465	4
540	29863	5
600	29195	6
620	28958	7
660	28462	8
697	27978	9
700	27938	10
770	26955	11
780	26808	12
852	25700	13
900	24916	14
941	24218	15
1020	22802	16
1100	21280	17
1140	20487	18
1209	19072	19
1300	17120	20
1336	16324	21
1380	15332	22
1477	13084	23
1500	12539	24
1620	9634	25
1633	9314	26
1700	7649	27
1740	6644	28
1860	3595	29
1980	514	30
2040	-1029	31
2100	-2570	32
2280	-7147	33
2400	-10125	34
2600	-14875	35
3825	-32457	36

FIG. 11C

Exemplary Call Progress Tones

Frequency1	Frequency2	Call Progress Tone
350	440	ANSI T1.401 dial tone
425	0	Q.35 Dial Tone
440	480	ANSI T1.401 audible ringing
480	620	ANSI T1.401 line busy tone
480	620	ANSI T1.401 Reorder
400	0	Audible ringing
440	0	Dial Tone
440	0	ANSI T1.401 Fast Busy Tone
440	0	Busy Tone

FIG. 11D

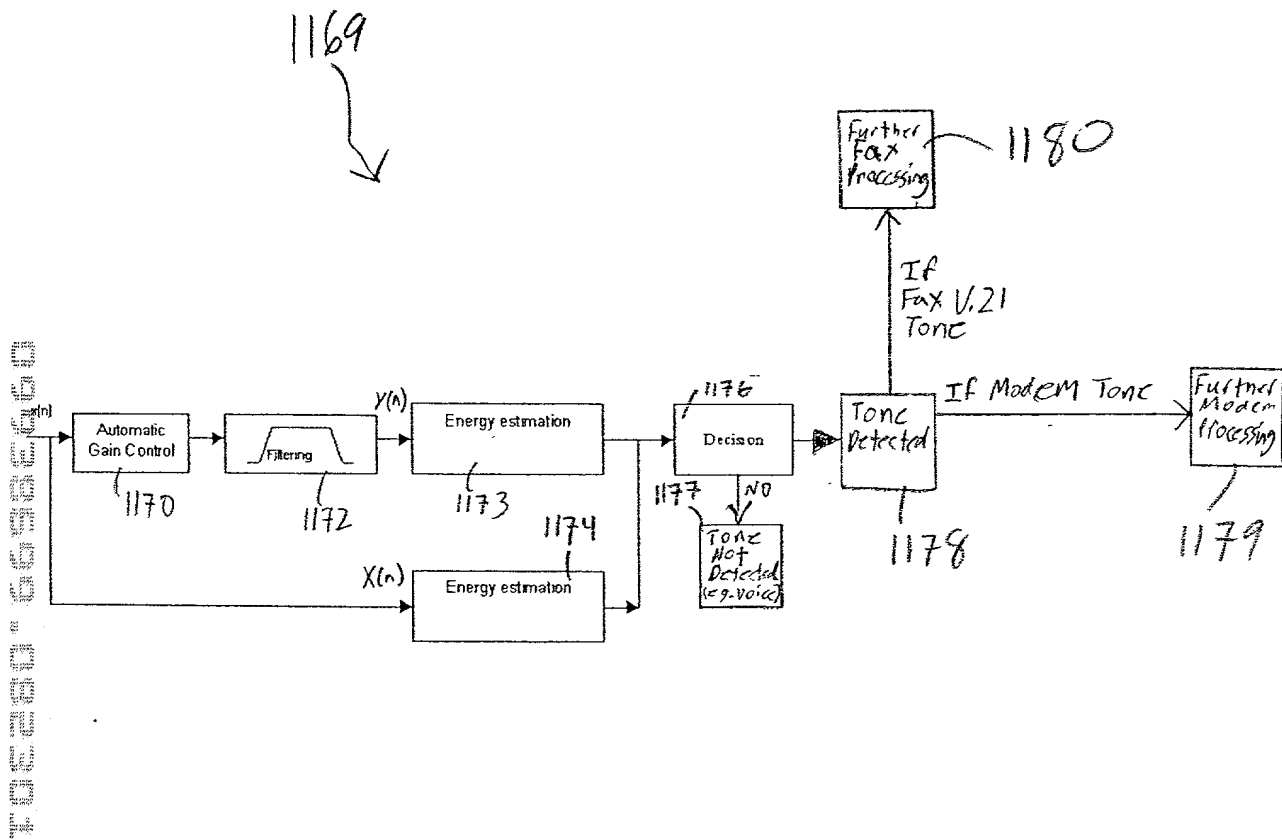


FIG. 11E

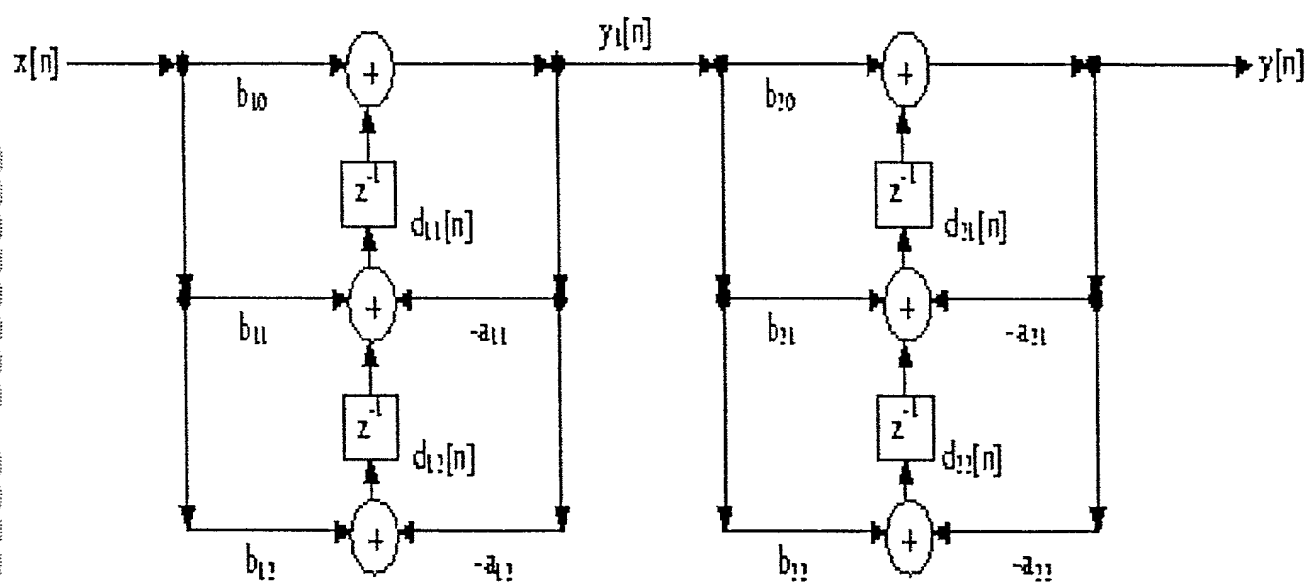


FIG. 11F

Method to detect Phase Reversals.

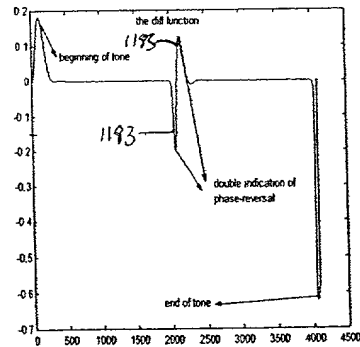
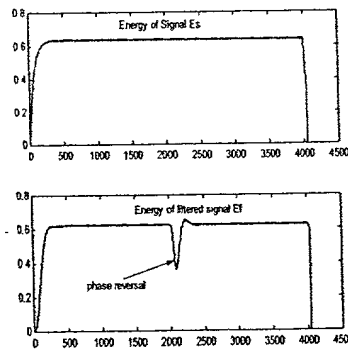
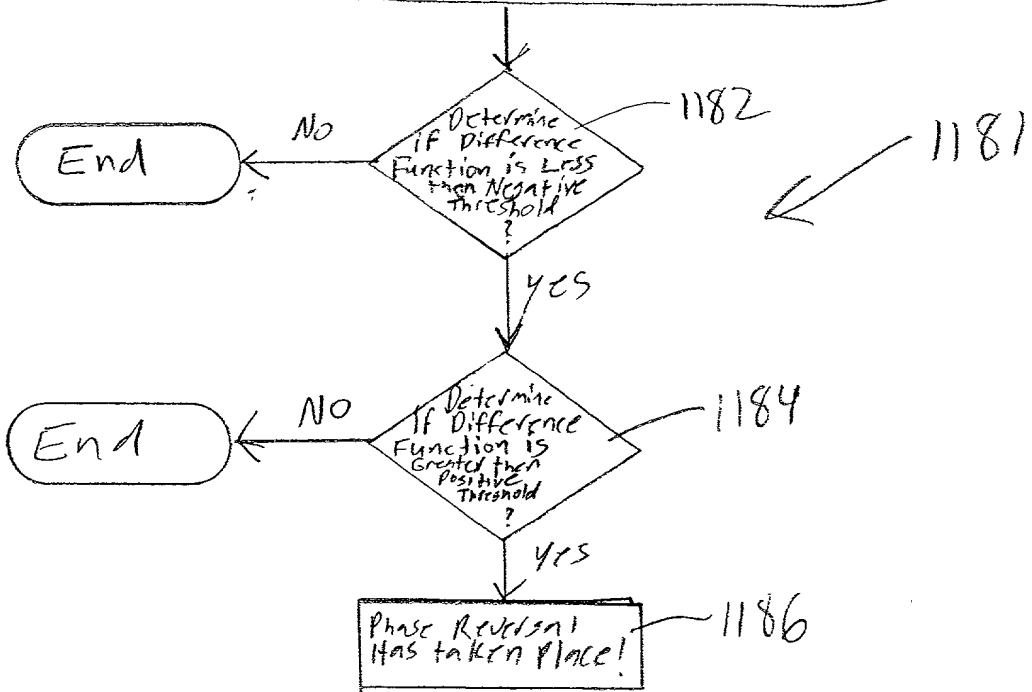


FIG. 116

Method for Fax V.21 Detection

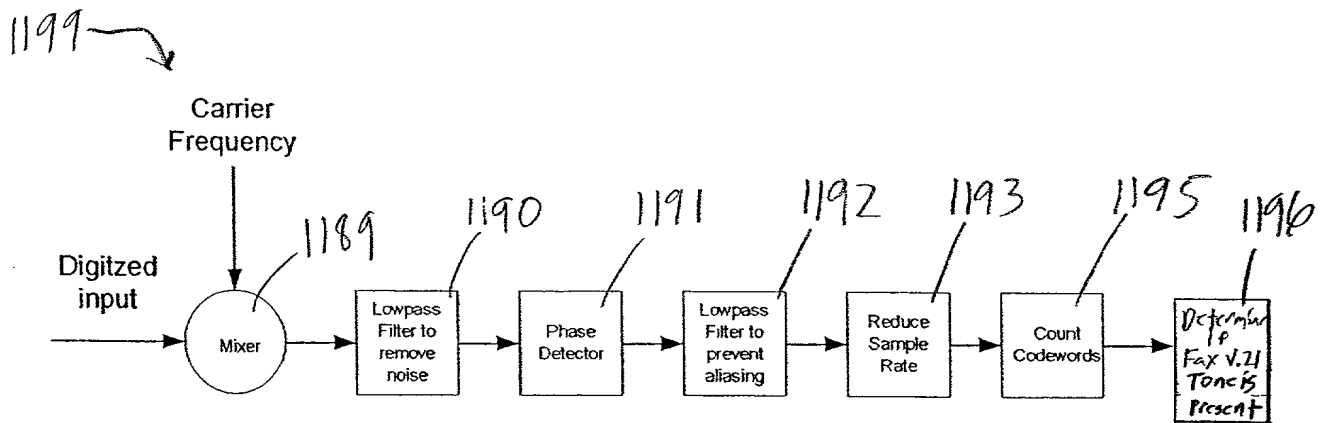


FIG. 11H

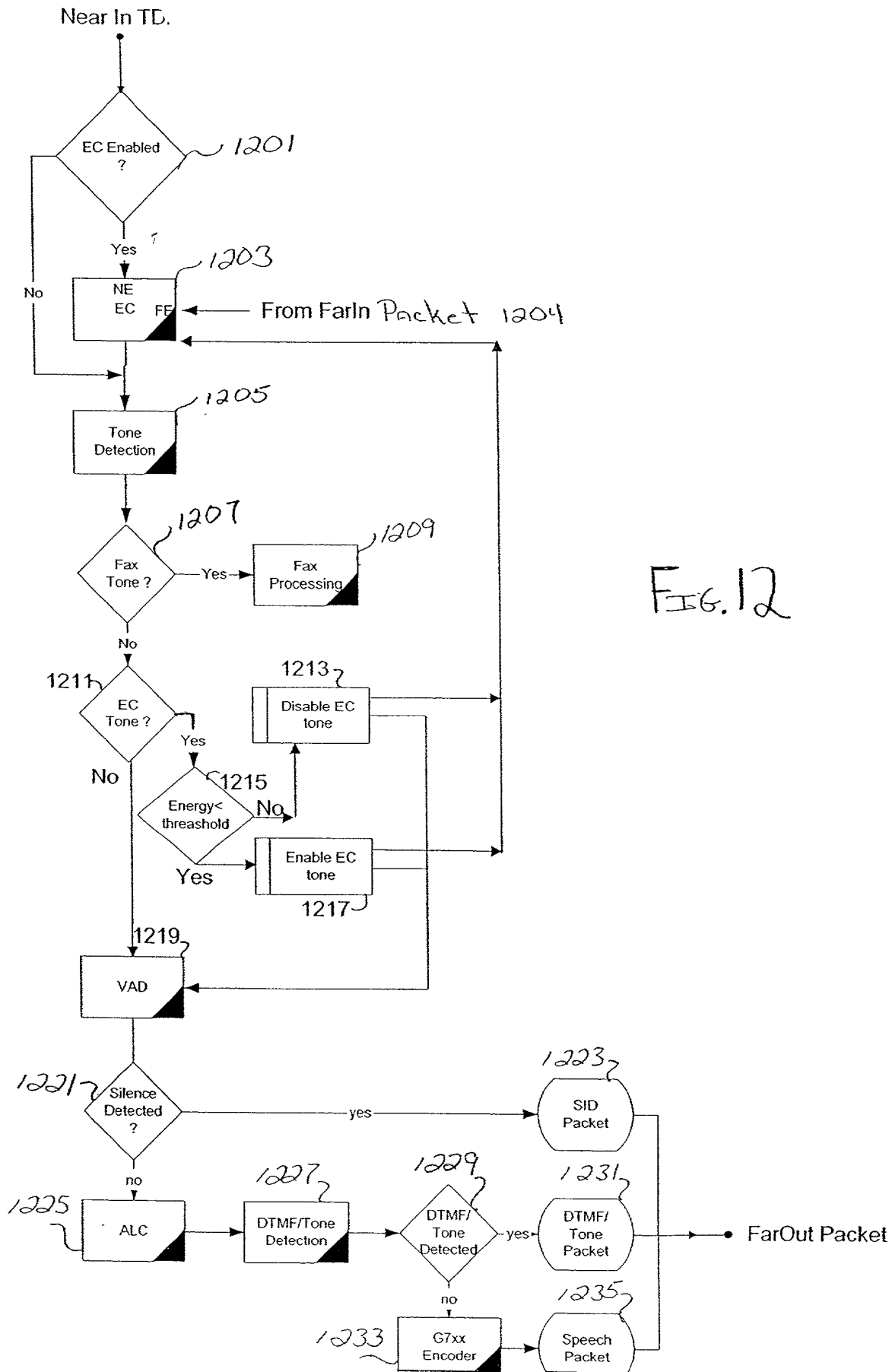


FIG. 12

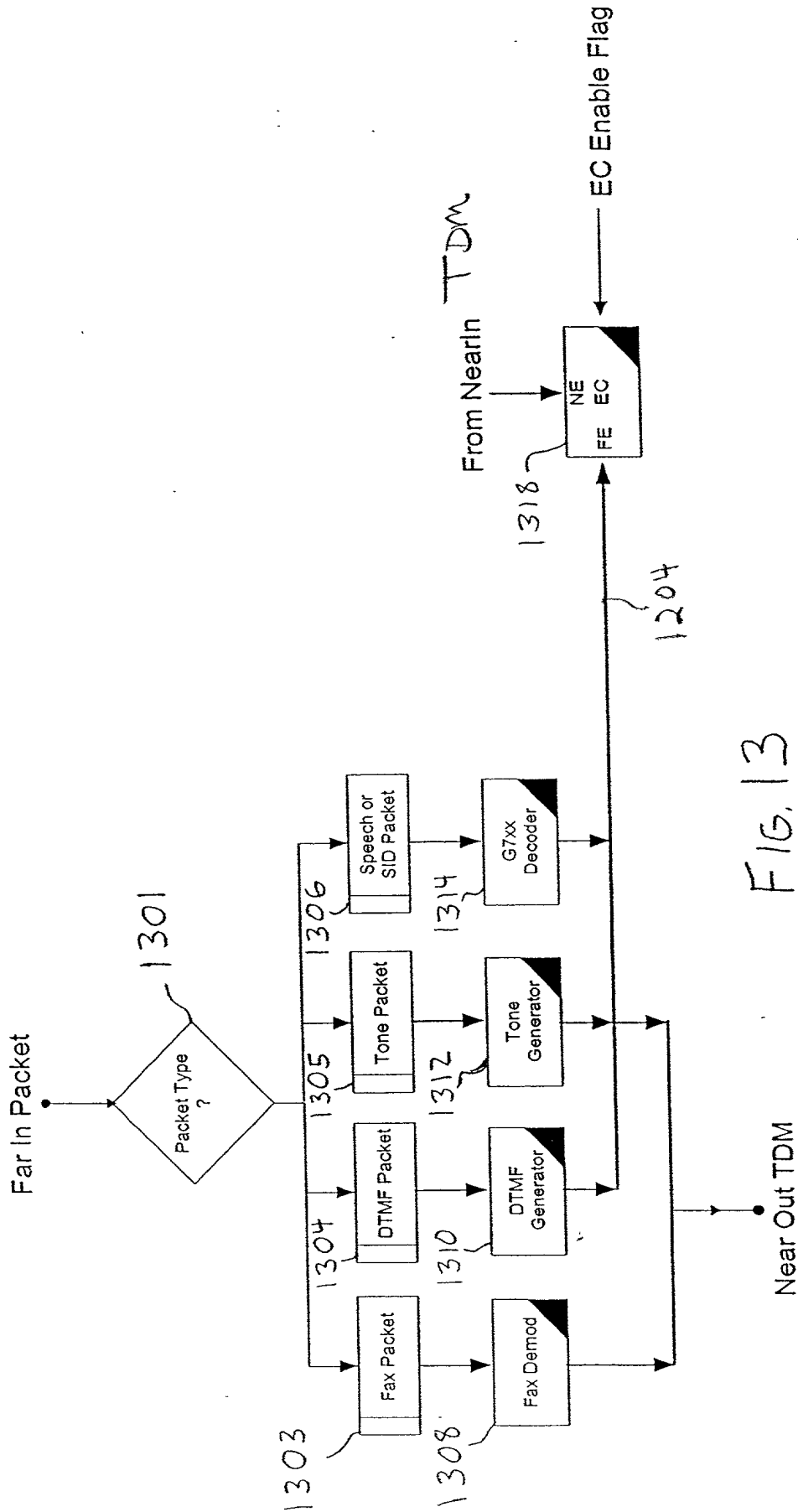


FIG. 13

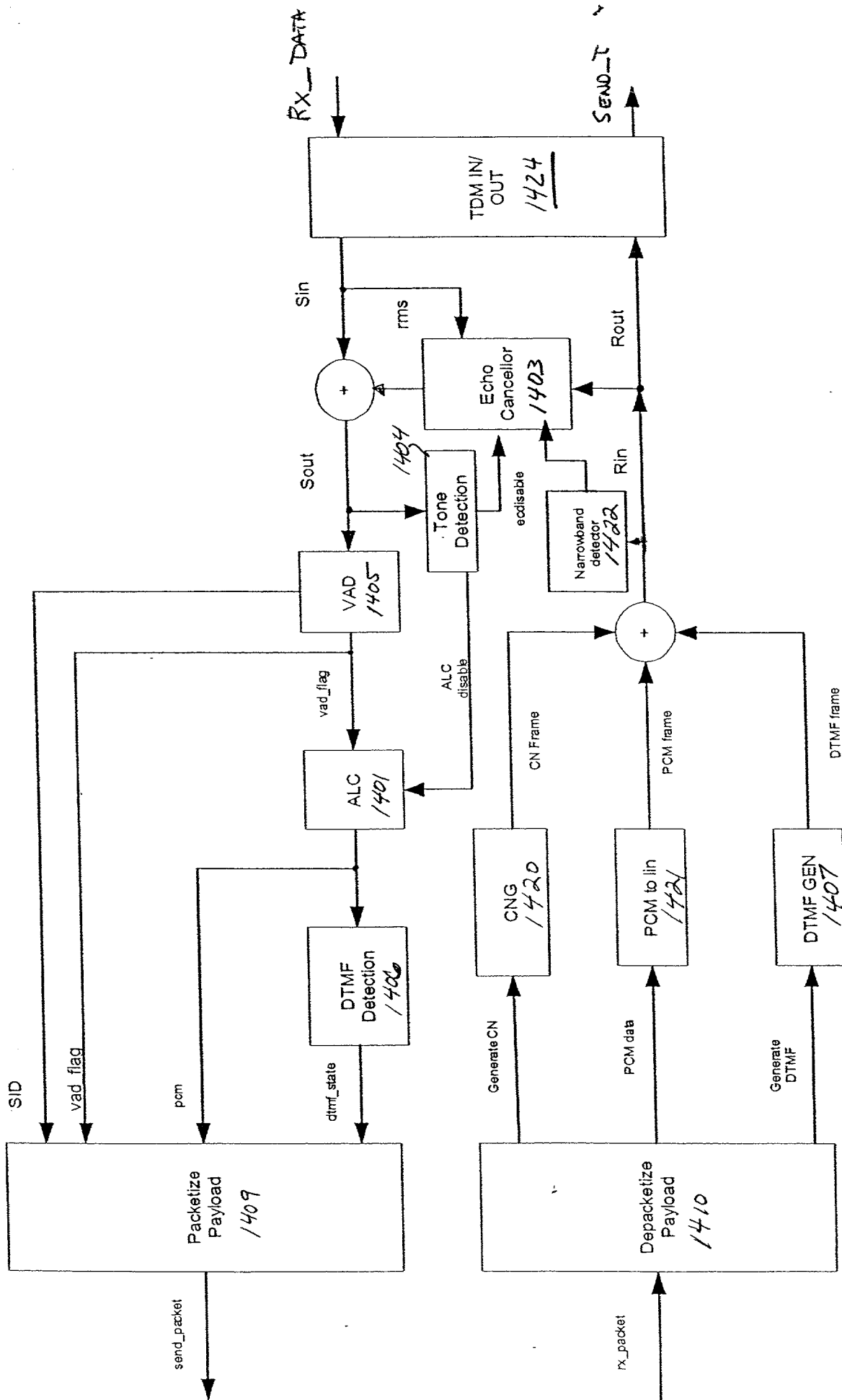
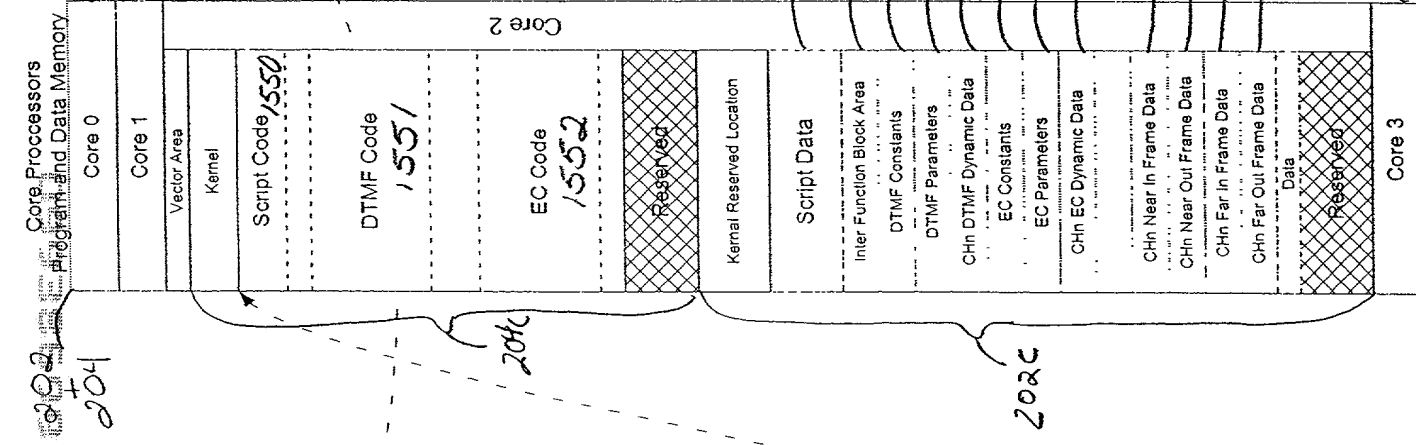
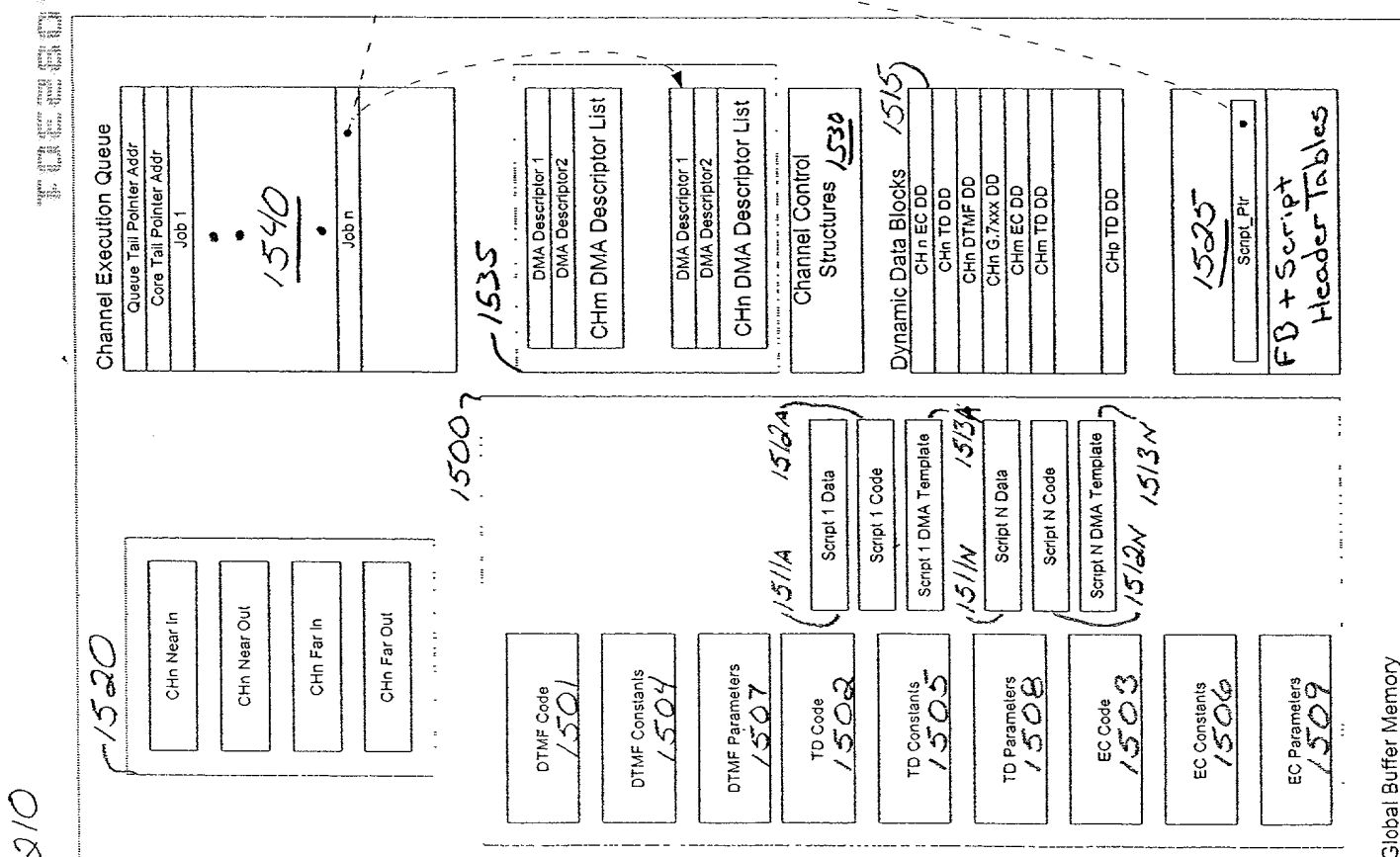


FIG. 14

210



413

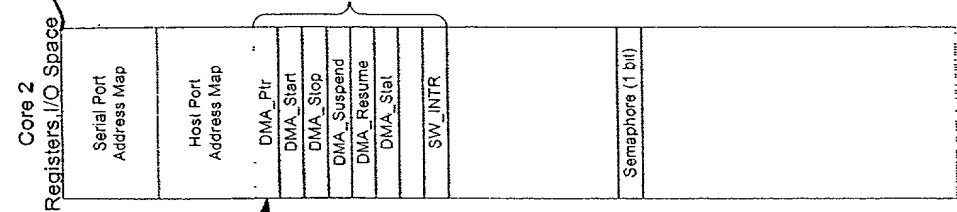


Fig. 15

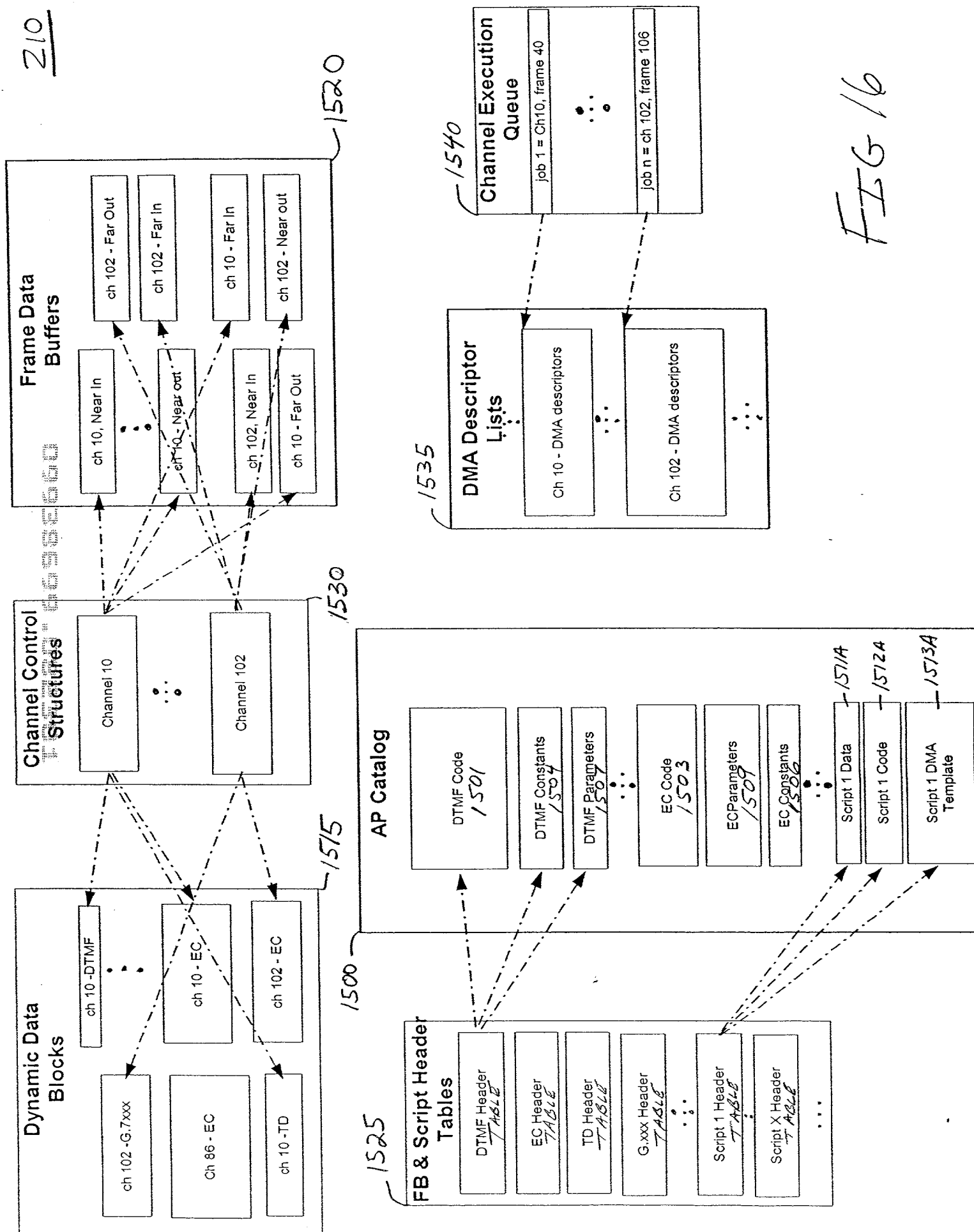


FIG 16

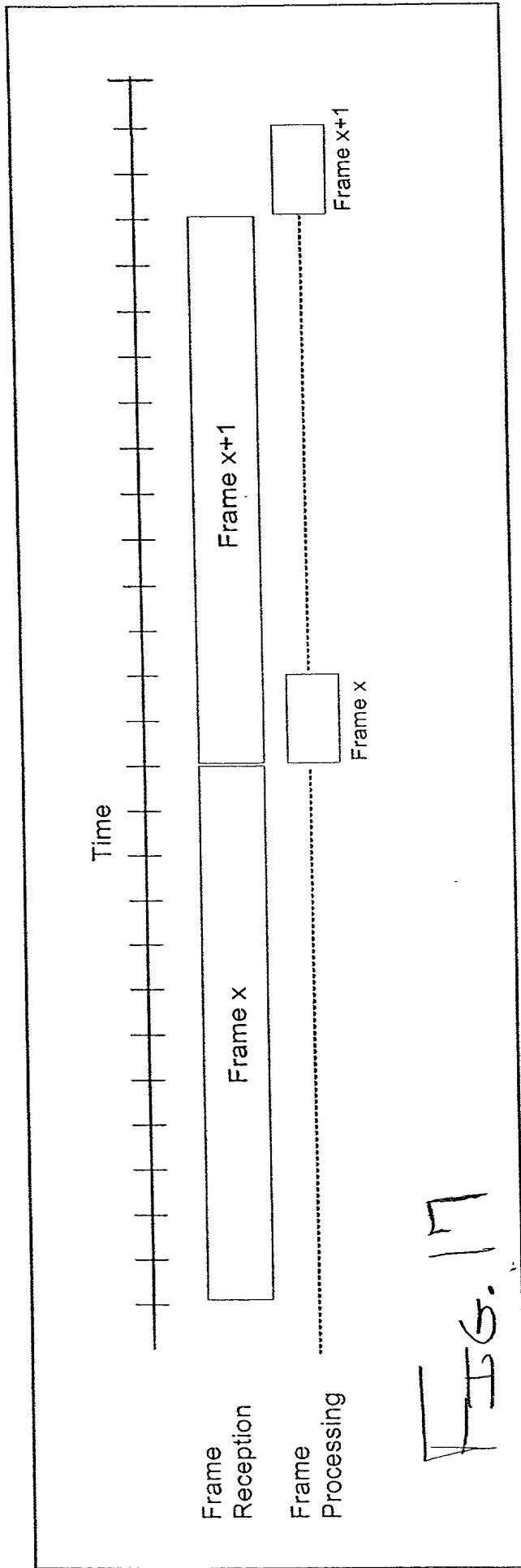


FIG. 17

FIG. 18

